Paper No. 32

UNITED STATES PATENT AND TRADEMARK OFFICE

_____

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

_____

Ex parte JAMES R. BUPP, DONALD S. FARQUHAR and LISA J. JIMAREZ

_____

Appeal No. 2001-1305
Application 08/872,782

_____

ON BRIEF

_____

Before THOMAS, KRASS, and FLEMING, **Administrative Patent Judges.**

FLEMING, **Administrative Patent Judge.**

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 12 and 17. Claims 13 through 16 have been withdrawn from consideration.

The invention relates to fabrication of an improved module which serves as an interconnecting platform between an integrated circuit chip and a card. See page 1 of Appellants' specification. Figure 1 is a cross section of an embodiment of

an organic carrier (card platform) mounting an I/C chip and mounted on a substrate according to the present invention. See page 6 of the Appellants' specification. Figure 1 shows dielectric layers 6 and 7, as well as dielectric layers 2 and 3. These dielectric layers are composite materials having a uoropolymer matrix, such as a PTFE matrix, containing, as a filler ingredient, ceramic particulate filler, such as silica (e.g., amorphous fused silica powder). See pages 7 and 8 of the Appellants' specification. Appellants recognize that the problem with these ceramic filler layers is that they allow corrosion when exposed to process chemicals such as resist strippers. See page 8 of Appellants' specification. Appellants solve this problem by providing PTFE layers 8 and 9. The PTFE barrier layers 8 and 9 are free of ceramic components and additives, such as silica or glass, and like materials which are not chemically inert to the presence of standard processing chemicals used to lipographically define fine line circuitry, electrical interconnection pads, and the like. The fluoropolymer barrier layers 8 and 9 consist essentially of fluoropolymer, i.e., while it is preferred to use a 100% pure fluoropolymer material in barrier layers 8 and 9, the presence of merely trace amounts of impurities of ceramics in layers 8 and 9 is also within the scope

of the invention, as long as the trace amounts of ceramic are not present in the amounts sufficient to sustain attack by process chemicals extensively enough to permit penetration of the process chemicals through the thickness of the barrier layer. See pages 8 and 9 of the Appellants' specification.

Independent claim 1 present in the application is reproduced as follows:

1. A packaging platform useful for interconnecting integrated circuit chips and cards, in which the platform comprises:

a circuitized laminate having opposite outer surfaces;

at least one ceramic-containing dielectric layer disposed on at least one of the opposite outer surfaces of said circuitized laminate.

at least one outermost protective impermeable fluoropolymer barrier layer devoid of ceramic material disposed on and covering said at least one ceramic containing dielectric layer, said outermost protective impermeable fluoropolymer barrier layer being impermeable to process chemicals encountered during fabrication of said integrated circuit chip and permitting metallized ceramic line processes without degradation of said integrated circuit chip;

at least one through hole extending between opposite outer surfaces of said laminate; and

a conductive material coating said at least one through hole.

References

The references relied on by the Examiner are as follows:

Bindra et al. (Bindra)	5,229,550	Jul. 20, 1993
Voss et al. (Voss)	4,830,704	May 16, 1989
Kametani (Japanes Patent)	2-186694	Jul. 20, 1990

Rejections at Issue

Claims 1 through 4 and 10 through 12 stand rejected under 35 U.S.C. § 103 as being unpatentable over Bindra in view of Kametani. Claims 5 through 9 and 17 stand rejected under 35 U.S.C. § 103 as being unpatentable over Bindra in view of Kametani and Voss.

Rather than repeat the arguments of the Appellants or the Examiner, we make reference to the brief and the answer for the respective details thereof.

OPINION

With full consideration being given to the subject matter on appeal, the Examiner's rejections and the arguments of Appellants and the Examiner, for the reasons state **infra**, we reverse the Examiner's rejection of claims 1 through 12 and 17 under 35 U.S.C. § 103.

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a **prima facie** case of obviousness. **In re Oetiker**, 977 F.2d 1443, 1445, 24 USPQ 1443, 1444 (Fed. Cir. 1992). **See also In re Piasecki**, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). The Examiner can satisfy this burden by showing that some objective teaching in the prior art or knowledge generally available to one of ordinary skill in the art suggests the claimed subject matter. **In re Fine**, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Only if this initial burden is met does the burden of coming forward with evidence or argument shift to the Appellants. **Oetiker**, 977 F.2d at 1445, 24 USPQ at 1444. **See also Piasecki**, 745 F.2d at 1472, 223 USPQ at 788.

An obviousness analysis commences with a review and consideration of all the pertinent evidence and arguments. "In reviewing the [E]xaminer's decision on appeal, the Board must necessarily weigh all of the evidence and arguments." **In re Oetiker**, 977 F.2d at 1445, 24 USPQ2d at 1444. "[T]he Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion." **In**

re Lee, 277 F.3d 1338, 1344, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002). With these principles in mind, we commence review of the pertinent evidence and arguments of Appellants and Examiner.

We first will address the rejection of claims 1 through 4 and 10 through 12 under 35 U.S.C. § 103 as being unpatentable over Bindra in view of Kametani. The Examiner has relied on Bindra for teaching all the claimed limitations except for the clearances between conductive material and conductive layers and the teaching of a chip. See page 4 of the Examiner's answer.

Appellants argue that Bindra does not teach or suggest

> [I]mpermeable fluoropolymer barrier layer devoid of ceramic material disposed on and covering at least one ceramic containing dielectric layer, said outermost protective impermeable fluoropolymer barrier layer being impermeable to process chemicals encountered during fabrication of said integrated circuit chip and permitting metallized ceramic line processes without degradation of said integrated circuit chip.

See page 5 of the brief. We note that this language is quoted from Appellants' claim 1. We further note that claim 10, the other independent claim, also recites similar language. Appellants argue that Bindra discloses that the inner dielectric material used for an insulating layer and the dielectric layer are formed from the same material. See pages 5 and 6 of the brief.

Upon our view of Bindra, we find that Bindra teaches in the background of the invention that the prior art high density circuit boards use a dielectric constant (Er) of about 3.2 or less, in order to reduce signal propagation delays and reduce signal noise and attenuation. See column 1, lines 37 through 50. Bindra further discloses that the prior art suitable materials which can be used to provide an Er of 3.2 or below. These suitable materials are fluorocarbons such as, for example, polytetrafluoroethylene (PTFE), polychlorotrifluoroethylene (CTFE), and polyperfluoropropylene, optionally filled with a filler, such as certain kinds of quartz or silicon particles. See column 2, lines 13 through 18. Bindra is concerned with the method or structure, wherein a dielectric material encapsulizes each high density wire core, and wherein encapsulated high density cores are aligned, using the joining material for alignment, to test on the subcomposite level and build for a high density printed circuit board or card. See column 3, lines 34 through 42.

Bindra discloses that figure 1 shows the best mode for carrying out the invention. In particular, figure 1A shows an encapsulated circuitized power core ready for joining to a like core. A dielectric material 1 is disposed on top the CPC, except

for the land and via areas. The via is filled and the land is coated with joining metal (2). The power core itself (3) is surrounded top and bottom with dielectric material (4), on which signal lines (5) are disposed. See column 5, lines 10 through 22.

Bindra then discloses the following experiments to indicate materials which have been used for making the encapsulated power core. The feasibility experiments were performed by using both a photosensitive dielectric approach and a non-photosensitive approach. The non-photosensitive material was a filled polytetrafluorethylene (PTFE) obtained from Rogers Corporation. See column 6, lines 6 through 14.

Bindra discloses the structures made using a non-photosensitive dielectric in column 7, line 44, to column 8, line 38. The only reference to the dielectric material used is found in column 7, lines 49 through 52, wherein Bindra discloses that the dielectric material is C. Roger 2810 and 2511 dielectrics.

Upon our review of the reference in its entirety, we fail to find any teaching or suggestion that two different dielectric materials would be used for dielectric element 4 and dielectric element 5 shown in figure 1A as alleged by the Examiner. In particular, we fail to find that Bindra teaches "at least one

ceramic-containing dielectric layer . . . at least one outermost protective impermeable fluorpolymer barrier layer devoid of ceramic material disposed on and covering said at least one ceramic containing dielectric layer, said outermost protective impermeable fluoropolymer barrier layer being impermeable to process chemicals encountered during fabrication of said integrated circuit chip and permitting metallized ceramic line processing without degradation of said integrated circuit chip" as set forth in Appellants' claim 1. Furthermore, we failed to find that Bindra teaches or suggests,

> a laminate having opposite outer surfaces and including at least one ceramic containing dielectric layer disposed and covering one of said opposite outer surfaces, said surfaces further comprising fine line circuitry and at least one outer most impermeable protective fluoropolymer barrier layer devoid of ceramic material wherein said outer most impermeable barrier layer covers said at least one ceramic-containing dielectric layer and is impermeable to process chemicals encountered during fabrication of said circuitized structure and permits metallized ceramic line processes without degradation of said circuitized structure;

as recited in Appellants' claim 10.

Therefore, we will not sustain the Examiner's rejection of claims 1 through 4 and 10 through 12 under 35 U.S.C. § 103 as being unpatentable over Bindra in view of Kametani.

We now turn to the rejection of claims 5 through 9 and 17 under 35 U.S.C. § 103 as being unpatentable over Bindra in view

of Kametani and Voss. We note that the Examiner relies on Bindra for a teaching of one ceramic-containing dielectric layer and a one outermost protective impermeable fluoropolymer layer devoid of ceramic material deposed on and covering said at least one ceramic containing dielectric layer. See page 5 of the Examiner's answer. We further note that claim 5 recites

> wherein said outermost and opposing outermost impermeable fluoropolymer barrier layers are devoid of ceramic components, and said first and second intermediate dielectric-layers comprise ceramic containing fluoropolymers, and
>
> wherein said outermost and opposing outermost impermeable fluoropolymer barrier layers are impermeable to process chemicals encountered during fabrication of said packaging platform and permit metallized ceramic line processes without degradation of said packaging platform.

Similarly, Appellants claim 10 recites

> a laminate having opposite outer surfaces and including at least one ceramic containing dielectric layer disposed and covering one of said opposite outer surfaces, said surface further comprising fine line circuitry and at least one outer most impermeable protective fluoropolymer barrier layer devoid of ceramic material wherein said outer most impermeable barrier layer covers said at least one ceramic-containing dielectric layer and is impermeable to process chemicals encountered during fabrication of said circuitized structure and permits metallized ceramic line processes without degradation of said circuitized structure.

Therefore, for the same reasons as we discussed above, we find that Bindra fails to teach these limitations.

In view of the foregoing, we have not sustained the Examiner's rejection of claims 1 through 12 and 17 under 35 U.S.C. § 103. Therefore, we reverse.

Reversed

JAMES D. THOMAS Administrative Patent Judge	)	
ERROL A. KRASS Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
MICHAEL R. FLEMING Administrative Patent Judge	)	

MRF:pgg

McGuire Woods, LLP
1750 Tysons Blvd
Suite 1800
Mclean, Virgina 22102-4215